A 12-Bit 50MS/s Pipelined ADC

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Abstract — A 12-Bit 50MHz ADC has been designed in TSMC 0.25um CMOS process with 1.8V power supply. The ADC used 11 stages of pipelined structure with fully differential circuits. Capacitor scaling technique was employed to reduce power consumption. The simulation achieved 66dB SNDR.

I. ARCHITECTURE

The block diagram of the pipelined ADC is shown in Fig. 1. It consists of an input sample and hold block and 11 stages. Each stage except for the last one contains a switched-capacitor MDAC and a 1.5-bit ADC. The last stage used the same 1.5-bit ADC. Compared to multi-bit per stage approach, 1.5-bit structure has the potential to achieve higher speed due to larger feedback factor (1/2), and for the same reason, the speed requirement of the op amps become less stringent.

However, 1.5-bit/stage structure will result in more latency. In this design, each stage only contribute half clock cycle latency to the digital bits output. In Fig. 2, the timing of the pipelined ADC is shown. Each stage operate on two non-overlapping clocks. During \( \Phi_1 \), stage 1 samples the output of the S&H block, and its 1.5-bit ADC quantizes that voltage. During \( \Phi_2 \), stage 1’s op amp will subtract the digital format signal from the input voltage, and stage 2 is sampling the result.

In each stage, it will generate two bit digital output. For the same input voltage, MSB (most significant bit) will come out first, and LSB (least significant bit) will come out last. A post DSP block is used to combine the 2-bit output of 11 stages into 12 bits. Due to the 1 bit redundancy in each stage, the digital output of stage 1 will be left shifted one bit and then added to the digital output of stage 2. The same rule applies to all stages.

II. DESIGN CONSIDERATION

A. Methodology

The SNDR required in this ADC is

\[
6.02 \times 12 + 1.76 = 74\text{dB}
\]

In this design, the top-to-bottom methodology was chosen to optimize the performance and power consumption. The performance of the pipelined ADC is mainly limited by thermal noise and non-linearity. By proper choice of sampling capacitor value, and proper design of the op amp and switches, the ADC can meet the performance goal with minimum power consumption. First, according to the SNDR requirement, the total input referred thermal noise can be derived, and using capacitor scaling, the power of later stages can be brought lower and lower due to smaller capacitor value. Second, knowing each stage’s sampling capacitor value, the DC bias current of its op amp and be derived to meet the required settling accuracy. Third, the DC open loop gain of the op amp in each stage must meet the requirement, in order not to bring significant non-linearity to the output. The later the stage, the lower the required op amp gain. Finally, the sampling switched in each stage is not ideal, due to finite on-resistance and non-linearity. The switch must settle within the given time, and better switch topology may be needed to give better linearity.
B. Thermal Noise

Suppose in the op amp design, the sum of Vds voltages of upper PMOS is 300mV and sum of Vds voltages of lower NMOS is also 300 mV. Due to the use of fully-differential op amps, the effective output swing is doubled,

\[ V_{FS} = 2 \times (1.8 - 0.3 - 0.3) = 2.4V \]

The SNDR requirement is 74dB, which is

\[
\text{SNDR} = 0.5 \times \left( \frac{V_{FS}}{2} \right)^2 = 10^{74/10} 
\]

Where \( V_n^2 \) is the total of thermal noise and non-linearity. Both of these two non-ideal factors must be limited below half of LSB value.

The quantization noise is

\[
Q_e = \frac{\text{LSB}^2}{12} = \frac{1}{12} \left( \frac{V_{FS}}{2} \right)^2 = 2.8 \times 10^{-8} 
\]

Therefore the total thermal noise has to be kept below

\[ V_n^2 < \frac{Q_e}{2} = 1.4 \times 10^{-8} \]

In switched-capacitor circuit, KT/C noise is the dominant thermal noise, and it has to be scaled properly in 11 stages. The input referred KT/C noise is

\[ V_n^2 = V_n^2 + \frac{V_n^2}{2} + \frac{V_n^2}{2^2} + \frac{V_n^2}{2^3} + \cdots \]

Since the number of stages is large, moderate scaling is needed. The contribution from each stage can be

\[ V_n^2 < \frac{V_n^2}{2} = 1.4 \times 10^{-8} \]

Suppose the noise from the first stage is

\[ V_{n1}^2 = \frac{KT}{C_1} = 7 \times 10^{-9} \]

\[ C_1 = 592fF \text{ round to 600fF} \]

And the noise and capacitor value of the following stages are

- stage 2: \( \frac{V_{n2}^2}{2^2} = \frac{V_{n1}^2}{2} \rightarrow C_2 = \frac{C_1}{2} = 300fF \)
- stage 3: \( \frac{V_{n3}^2}{2^3} = \frac{V_{n2}^2}{2} \rightarrow C_3 = \frac{C_1}{2^2} = 150fF \)
- stage 4: \( \frac{V_{n4}^2}{2^4} = \frac{V_{n3}^2}{2^2} \rightarrow C_4 = \frac{C_1}{2^3} = 100fF \)
- stage n: \( C_n = \frac{C_1}{2^n-1} = 100fF \)

Start on stage 4, capacitor scaling stops at 100fF for better matching in layout.

C. Effective Load Capacitance Estimation

In Fig. 3, the load capacitance is estimated.

\[ C_{L,\text{eff}} = \left( \frac{C_s + C_p}{C_s + C_p + C_s + C_{\text{ADC}}} + C_{\text{next}} \right) \]

This is estimated as \( C_{L,\text{eff}} = 3C_s \).

D. Op Amp Open Loop Gain Requirement

According to well-established result, the open loop gain of op amp in each stage is

- 1st stage: \( A_o > 2^{12} = 73dB \), design for better than 80dB
- 2nd stage: \( A_o > 2^{11} = 67dB \), design for better than 74dB
- 3rd stage: \( A_o > 2^{10} \), design for better than 68dB
- 4th stage: \( A_o > 2^9 \), design for better than 62dB
- …
- 10th stage: \( A_o > 2^3 \), design for better than 26dB

The first stage op amp has the most stringent gain requirement. In this design, telescopic op amp was chosen and gain-boosting technique was used to achieve high gain.

E. Op Amp Settling Requirement

For the first stage op amp, it has to settle to better than half of LSB.

\[ \text{err} = \exp \left( -\frac{T_s/2}{\tau} \right) = \frac{\text{LSB}/2}{V_{FS}} = 0.5 \times 2^{12} = 1.22 \times 10^{-4} \]

Where \( \tau = 10ns/9.01 = 1.11ns \) determined the GBW,

\[ \frac{1}{\tau} = \frac{\beta g_m}{C_L} = 900MHz \]
The feedback factor $\beta$ is 0.5 ideally, but taking parasitic capacitance into account, the $\beta$ is approximately 0.3–0.4. In this design, $\beta \approx 0.3$ is chosen for worst case.

For the following stages,

$$\text{err} = \exp\left(-\frac{\tau}{2}\right) < \frac{0.5}{2^{13-n}} \text{ for nth stage}$$

For the first stage, the DC bias current can be calculated as,

$$\frac{0.3 \times g_m}{3 \times 600fF} = 900MHz$$

$$g_m = 5.4m \frac{V}{\sqrt{A \times V_{dd}}}$$

For the input transistor, the over drive voltage is chosen close to 100mV. So the DC current is 270uA.

**F. Op Amp Slewing Requirement**

For the first stage,

$$SR = \frac{V_{op} - V_{on}}{\Delta t} = \frac{2I_D}{C_L}$$

$$V_{op} - V_{on} = 1.8 - 0.3 - 0.3 = 1.2V$$

$$\Delta t = T_s/2/10 = 1ns, \ C_L = 3C_s = 1.8pF$$

So in order to satisfy slewing requirement, the DC current has to be greater than 270uA, and it should be at least $I_D = 1mA$.

**G. Switch Settling and Linearity Requirement**

The on-resistance must be chosen to meet the settling requirement. During the sampling phase, the sampling capacitor and the switch will be equivalent to R and C in series. For N-bit settling accuracy, and sampling clock period of $T_s$, the following relation has to be met

$$\exp\left[-\frac{0.5T_s}{R_{on}C_s}\right] < 0.5$$

Which means it has to settle to the accuracy twice better than the requirement within half clock period when the clock signal is high.
For the first stage switch,
\[
\exp \left[ -\frac{0.5 \times 20n}{R_{on} \times 600fF} \right] \leq \frac{0.5}{2^{12}}
\]
The on-resistance of the switch should be less than Ron=1.8k.
The following stages will be scaled in a similar way.

For the sampling switches, small on-resistance alone cannot guarantee accuracy, its linearity also matters. In Fig. 6, two kinds of switch are shown. They are T-gate (transmission gate) and bootstrap switch. T-gate has the advantage of simplicity, but its on-resistance depends on the input signal because of transistor’s body effect.

Bootstrap switch can use a charge pump to keep the VGS voltage of the sampling transistor always equal to Vdd, therefore guarantee excellent linearity. Given the linearity requirement of this pipelined ADC, the first 4 stages used bootstrap switches to sampling their input signal, and the rest of stages used T-gates.

III. OP AMP DESIGN

In order to get more than 80dB gain and also high gain-bandwidth product, gain-boosted telescopic op amp topology is chosen. Gain-boosting is a technique to decouple gain and speed requirement. In Fig. 4, the schematic is shown. M1~M8 need to support large current 1mA, therefore high speed is achieved with the sacrifice of lower gain.

But the N-booster and P-booster can increase the overall op amp gain by a factor of the booster gain. And the booster doesn’t need to be very high speed, their GBW product only need to be much greater than the non-dominant pole of the op amp.

In Fig.4, the desired output common-mode voltage of the two boosters VB2 and VB5 are provided by the biasing network. Especially, VB5 is designed to track the virtual ground node voltage VGND.

For boosting M5~M6, an op amp with NMOS input is needed because the drain voltage of M7~M8 is close to Vdd. For similar reason, M3~M4 need an op amp with PMOS input. The N-booster and P-booster are shown in Fig. 5.

IV. SUB-ADC DESIGN

A. Fully-differential Comparator

Fig.7 and Fig.8 show the comparator schematic and its timing. The requirement of low latency in the ADC demands the comparator to finish its job in the non-overlapping period.
B. 1.5-bit ADC

The sub-ADC used two fully-differential comparators to achieve three levels. Two resistor ladders are used to decouple the interference from each other. Ru is the unit resistor in the ladder, its value is chosen to meet settling requirement. The reference voltages are set to Vdd-300mV=1.5V and 300mV, in order not to saturate the op amps.

V. MDAC

The MDAC stage uses the op amp designed in Part III to subtract the digital form input signal from its original analog input signal. The following equation is realized in MDAC,

\[ V_{\text{out}} = 2V_{\text{in}} - V_{\text{dac}} \]

As shown in Fig.8, at the end of phi2, the 1.5-bit ADC start to read the input signal and compare it with the two reference voltages provided by the resistor ladder. And the same time, the MDAC finished sampling of the input signal on the two sampling capacitors Cs. This ensures that the signal stored on Cs is the same signal being quantized by the 1.5-bit ADC, and therefore it does not need a S&H block any more.

Before the rising edge of phi1, the digital output of the 1.5-bit ADC is already available, so when phi1 goes high, the op amp will perform the subtraction of the digital signal from its original analog signal stored in the capacitors.

VI. FIRST STAGE S&H

Although each stage doesn’t need any S&H because of the advanced timing scheme chosen in this design, the first stage still need S&H due to the changing of the input signal.

The S&H block in Fig.11 will hold the signal unchanged for half clock period during the operation of the next stage. The sampling switch here needs to be bootstrap switch to provide high linearity for the first stage. The op amp here, however, does not need to have high gain, because finite op amp gain will only bring gain error to the output, not non-linearity.

VII. POST DIGITAL PROCESSING

In Fig. 1, the 11 2-bit output from all the stages need to be combined in a way to provide the 12-bit final digital output. Fig. 13 shows the structure of the post DSP block. And Fig. 12 shows the method to combine those outputs.

Since the latency resulted from one stage is half clock period, the previous stage’s output needs to be delayed by half clock period and added to the next stage output. Each delay line consists of a lot of D-flip-flops, clocking on phi1, phi2, phi1, phi2, …… alternatively to provide the required delay to the digital output codes. At the end of the delay line, a thermometer to binary encoder convert the output to binary code. Then they are added together in the way shown in Fig. 12 to get the final 12-bit output.
Fig. 13 Post Digital Processing
VIII. SIMULATION

A. Ramp Input

In Fig. 14, a ramp from 300mV to 1.5V is applied to the pipelined ADC. An ideal 12-bit DAC is used to reconstruct the digital output to its analog form. The simulation result shows there is no missing code.

In Fig. 15, a much slower ramp is applied to the input, to show the steps around 1.25V. As required by the project, the output residue of the second stage is shown in Fig. 16, it is the same as the residue of a 2.5-bit stage.

B. Sine-wave Input

In Fig. 17, full scale sine input signals with two frequency are simulated. It is shown that SNDR of 66.3dB was achieved. Because of the use of fully-differential circuit, the even-order harmonics are suppressed. It can also be shown that for input frequency close to Nyquist frequency, high order harmonics are aliased to low frequencies.